



## 3.3V CMOS 18-BIT REGISTERED BUS TRANSCEIVER WITH 5V TOLERANT I/O AND BUS-HOLD

**IDT74LVCH16501A**

### FEATURES:

- Typical  $t_{sk(o)}$  (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{CC} = 3.3V \pm 0.3V$ , Normal Range
- $V_{CC} = 2.7V$  to  $3.6V$ , Extended Range
- CMOS power levels ( $0.4\mu W$  typ. static)
- All inputs, outputs, and I/O are 5V tolerant
- Supports hot insertion
- Available in SSOP, TSSOP, and TVSOP packages

### DRIVE FEATURES:

- High Output Drivers:  $\pm 24mA$
- Reduced system switching noise

### APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

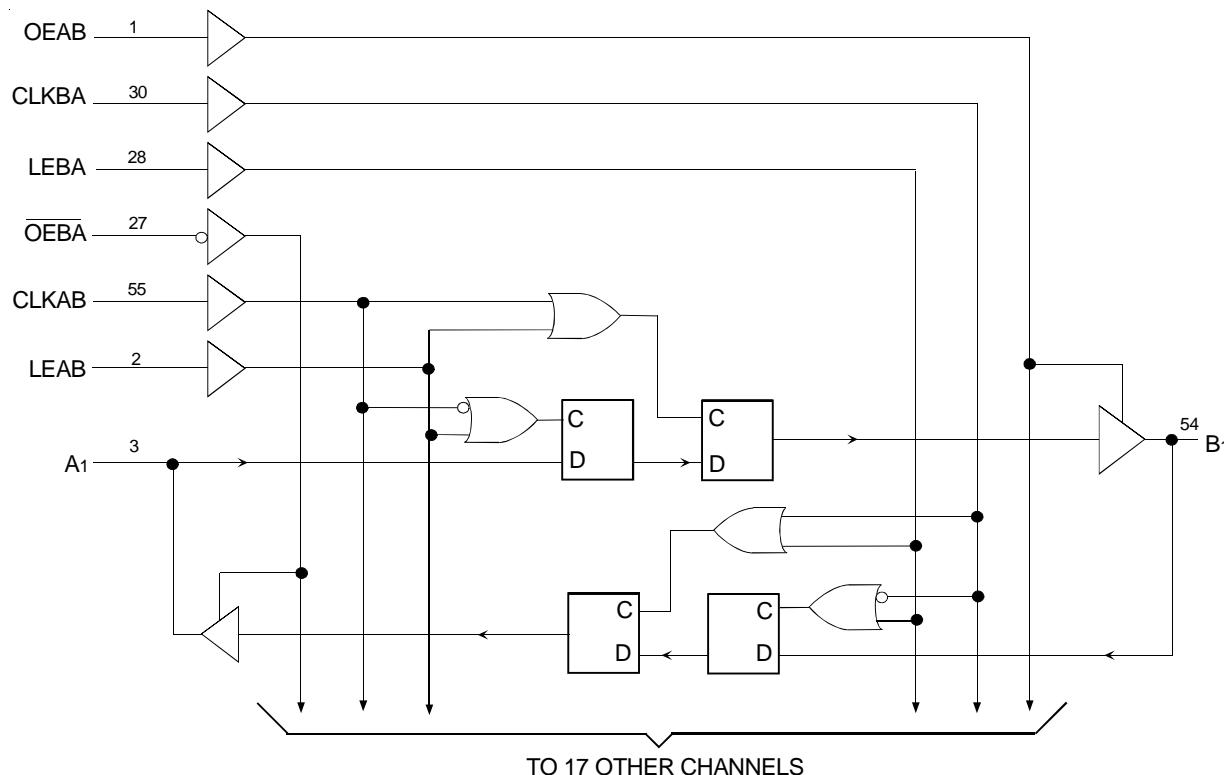
### DESCRIPTION:

This 18-bit registered transceiver is built using advanced dual metal CMOS technology. This high-speed, low power 18-bit registered bus transceiver combines D-type latches and D-type flip-flops to allow data flow in transparent latched and clocked modes. Data flow in each direction is controlled by output-enable (OEAB and  $\overline{OEBA}$ ), latch enable (LEAB and LEBA) and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. OEAB performs the output enable function on the B port. Data flow from B port to A port is similar but requires using  $\overline{OEBA}$ , LEBA and CLKBA. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The LVCH16501A has been designed with a  $\pm 24mA$  output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The LVCH16501A has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

### FUNCTIONAL BLOCK DIAGRAM



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INDUSTRIAL TEMPERATURE RANGE

OCTOBER 1999

## PIN CONFIGURATION

OEAB	1	56	GND
LEAB	2	55	CLKAB
A1	3	54	B1
GND	4	53	GND
A2	5	52	B2
A3	6	51	B3
Vcc	7	50	Vcc
A4	8	49	B4
A5	9	48	B5
A6	10	47	B6
GND	11	46	GND
A7	12	45	B7
A8	13	44	B8
A9	14	43	B9
A10	15	42	B10
A11	16	41	B11
A12	17	40	B12
GND	18	39	GND
A13	19	38	B13
A14	20	37	B14
A15	21	36	B15
Vcc	22	35	Vcc
A16	23	34	B16
A17	24	33	B17
GND	25	32	GND
A18	26	31	B18
OEBA	27	30	CLKBA
LEBA	28	29	GND

SSOP/ TSSOP/ TVSOP  
TOP VIEW

## PIN DESCRIPTION

Pin Names	Description
OEAB	A-to-B Output Enable Input
OEBA	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
Ax	A-to-B Data Inputs or B-to-A 3-State Outputs <sup>(1)</sup>
Bx	B-to-A Data Inputs or A-to-B 3-State Outputs <sup>(1)</sup>

## NOTE:

1. These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description	Max	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +6.5	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-50 to +50	mA
IIK	Continuous Clamp Current, $VI < 0$ or $VO < 0$	-50	mA
IOK			
Icc	Continuous Current through each Vcc or GND	±100	mA
Iss			

## NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE ( $TA = +25^\circ\text{C}$ ,  $F = 1.0\text{MHz}$ )

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
$C_{IN}$	Input Capacitance	$V_{IN} = 0\text{V}$	4.5	6	pF
$C_{OUT}$	Output Capacitance	$V_{OUT} = 0\text{V}$	6.5	8	pF
$C_{I/O}$	I/O Port Capacitance	$V_{IN} = 0\text{V}$	6.5	8	pF

## NOTE:

1. As applicable to the device type.

FUNCTION TABLE<sup>(1,2)</sup>

Inputs				Output
OEAB	LEAB	CLKAB	Ax	Bx
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	L	X	B <sup>(3)</sup>
H	L	H	X	B <sup>(4)</sup>

## NOTES:

1. A-to-B data flow is shown. B-to-A data flow is similar, but uses OEBA, LEBA, and CLKBA.
2. H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
Z = High-Impedance  
↑ = LOW-to-HIGH Transition
3. Output level before the indicated steady-state input conditions were established.
4. Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition:  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ 

Symbol	Parameter	Test Conditions		Min.	Typ. <sup>(1)</sup>	Max.	Unit
V <sub>IH</sub>	Input HIGH Voltage Level	V <sub>CC</sub> = 2.3V to 2.7V		1.7	—	—	V
		V <sub>CC</sub> = 2.7V to 3.6V		2	—	—	
V <sub>IL</sub>	Input LOW Voltage Level	V <sub>CC</sub> = 2.3V to 2.7V		—	—	0.7	V
		V <sub>CC</sub> = 2.7V to 3.6V		—	—	0.8	
I <sub>IH</sub> I <sub>IL</sub>	Input Leakage Current	V <sub>CC</sub> = 3.6V	V <sub>I</sub> = 0 to 5.5V	—	—	$\pm 5$	$\mu\text{A}$
I <sub>OZH</sub> I <sub>OZL</sub>	High Impedance Output Current (3-State Output pins)	V <sub>CC</sub> = 3.6V	V <sub>O</sub> = 0 to 5.5V	—	—	$\pm 10$	$\mu\text{A}$
I <sub>OFF</sub>	Input/Output Power Off Leakage	V <sub>CC</sub> = 0V, V <sub>IN</sub> or V <sub>O</sub> $\leq$ 5.5V		—	—	$\pm 50$	$\mu\text{A}$
V <sub>IK</sub>	Clamp Diode Voltage	V <sub>CC</sub> = 2.3V, I <sub>IN</sub> = -18mA		—	-0.7	-1.2	V
V <sub>H</sub>	Input Hysteresis	V <sub>CC</sub> = 3.3V		—	100	—	mV
I <sub>CCL</sub> I <sub>CCH</sub> I <sub>CCZ</sub>	Quiescent Power Supply Current	V <sub>CC</sub> = 3.6V	V <sub>IN</sub> = GND or V <sub>CC</sub>	—	—	10	$\mu\text{A}$
			3.6 $\leq$ V <sub>IN</sub> $\leq$ 5.5V <sup>(2)</sup>	—	—	10	
$\Delta I_{CC}$	Quiescent Power Supply Current Variation	One input at V <sub>CC</sub> - 0.6V, other inputs at V <sub>CC</sub> or GND		—	—	500	$\mu\text{A}$

## NOTES:

1. Typical values are at V<sub>CC</sub> = 3.3V,  $+25^\circ\text{C}$  ambient.

2. This applies in the disabled state only.

## BUS-HOLD CHARACTERISTICS

Symbol	Parameter <sup>(1)</sup>	Test Conditions		Min.	Typ. <sup>(2)</sup>	Max.	Unit
I <sub>BHH</sub> I <sub>BHL</sub>	Bus-Hold Input Sustain Current	V <sub>CC</sub> = 3V	V <sub>I</sub> = 2V	-75	—	—	$\mu\text{A}$
			V <sub>I</sub> = 0.8V	75	—	—	
I <sub>BHH</sub> I <sub>BHL</sub>	Bus-Hold Input Sustain Current	V <sub>CC</sub> = 2.3V	V <sub>I</sub> = 1.7V	—	—	—	$\mu\text{A}$
			V <sub>I</sub> = 0.7V	—	—	—	
I <sub>BHHO</sub> I <sub>BHLO</sub>	Bus-Hold Input Overdrive Current	V <sub>CC</sub> = 3.6V	V <sub>I</sub> = 0 to 3.6V	—	—	$\pm 500$	$\mu\text{A}$

## NOTES:

1. Pins with Bus-Hold are identified in the pin description.

2. Typical values are at V<sub>CC</sub> = 3.3V,  $+25^\circ\text{C}$  ambient.

## OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = 2.3V to 3.6V	IOH = - 0.1mA	VCC - 0.2	—	V
		VCC = 2.3V	IOH = - 6mA	2	—	
		VCC = 2.3V	IOH = - 12mA	1.7	—	
		VCC = 2.7V		2.2	—	
		VCC = 3V		2.4	—	
		VCC = 3V	IOH = - 24mA	2	—	
VOL	Output LOW Voltage	VCC = 2.3V to 3.6V	IOL = 0.1mA	—	0.2	V
		VCC = 2.3V	IOL = 6mA	—	0.4	
			IOL = 12mA	—	0.7	
		VCC = 2.7V	IOL = 12mA	—	0.4	
		VCC = 3V	IOL = 24mA	—	0.55	

NOTE:

1.  $V_{IH}$  and  $V_{IL}$  must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate  $V_{CC}$  range.  
 $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

## OPERATING CHARACTERISTICS, $V_{CC} = 3.3V \pm 0.3V$ , $T_A = 25^\circ\text{C}$

Symbol	Parameter	Test Conditions	Typical	Unit
CPD	Power Dissipation Capacitance per Transceiver Outputs enabled	$C_L = 0\text{pF}$ , $f = 10\text{MHz}$		$\text{pF}$
CPD	Power Dissipation Capacitance per Transceiver Outputs disabled			

SWITCHING CHARACTERISTICS<sup>(1)</sup>

Symbol	Parameter	V <sub>CC</sub> = 2.7V		V <sub>CC</sub> = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	
t <sub>PLH</sub>	Propagation Delay Ax to Bx or Bx to Ax	1.5	5.2	1.5	4.6	ns
t <sub>PHL</sub>	Propagation Delay LEBA to Ax, LEAB to Bx	1.5	6	1.5	5.3	ns
t <sub>PLH</sub>	Propagation Delay CLKBA to Ax, CLKAB to Bx	1.5	6	1.5	5.3	ns
t <sub>PZH</sub>	Output Enable Time OEBA to Ax, OEAB to Bx	1.5	6	1.5	5.6	ns
t <sub>PHZ</sub>	Output Disable Time OEBA to Ax, OEAB to Bx	1.5	6.5	1.5	5.8	ns
t <sub>su</sub>	Set-up Time, HIGH or LOW Ax to CLKAB, Bx to CLKBA	3	—	3	—	ns
t <sub>H</sub>	Hold Time, HIGH or LOW Ax to CLKAB, Bx to CLKBA	0	—	0	—	ns
t <sub>su</sub>	Set-up Time, HIGH or LOW Ax to LEAB, Bx to LEBA	3	—	3	—	ns
		2	—	2	—	
t <sub>H</sub>	Hold Time, HIGH or LOW Ax to LEAB, Bx to LEBA	1.5	—	1.5	—	ns
t <sub>w</sub>	Pulse Width HIGH, LEAB or LEBA	3	—	3	—	ns
t <sub>w</sub>	Pulse Width HIGH or LOW, CLKAB or CLKBA	3	—	3	—	ns
t <sub>sk(0)</sub>	Output Skew <sup>(2)</sup>	—	—	—	500	ps

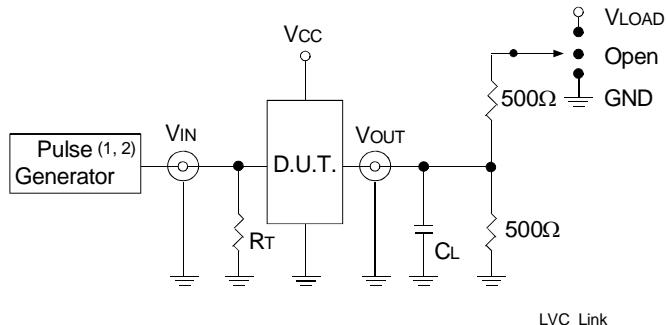
## NOTES:

1. See TEST CIRCUITS AND WAVEFORMS. TA = -40°C to +85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

## TEST CIRCUITS AND WAVEFORMS

## TEST CONDITIONS

Symbol	$V_{CC}^{(1)} = 3.3V \pm 0.3V$	$V_{CC}^{(1)} = 2.7V$	$V_{CC}^{(2)} = 2.5V \pm 0.2V$	Unit
$V_{LOAD}$	6	6	$2 \times V_{CC}$	V
$V_{IH}$	2.7	2.7	$V_{CC}$	V
$V_T$	1.5	1.5	$V_{CC} / 2$	V
$V_{LZ}$	300	300	150	mV
$V_{HZ}$	300	300	150	mV
$C_L$	50	50	30	pF



Test Circuit for All Outputs

## DEFINITIONS:

$C_L$  = Load capacitance: includes jig and probe capacitance.

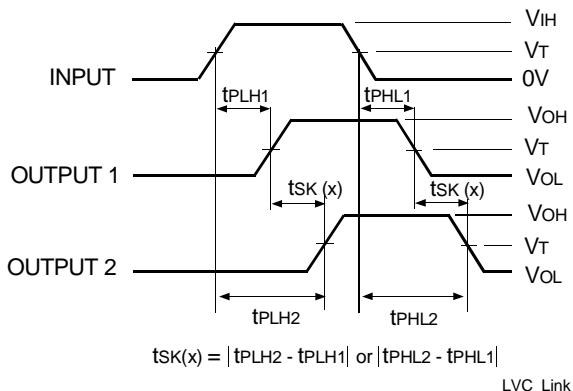
$R_T$  = Termination resistance: should be equal to  $Z_{OUT}$  of the Pulse Generator.

## NOTES:

1. Pulse Generator for All Pulses: Rate  $\leq 10MHz$ ;  $t_f \leq 2.5ns$ ;  $t_r \leq 2.5ns$ .
2. Pulse Generator for All Pulses: Rate  $\leq 10MHz$ ;  $t_f \leq 2ns$ ;  $t_r \leq 2ns$ .

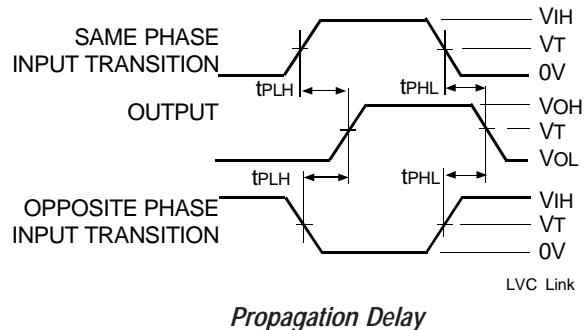
## SWITCH POSITION

Test	Switch
Open Drain	$V_{LOAD}$
Disable Low	
Enable Low	
Disable High	$GND$
Enable High	
All Other Tests	Open

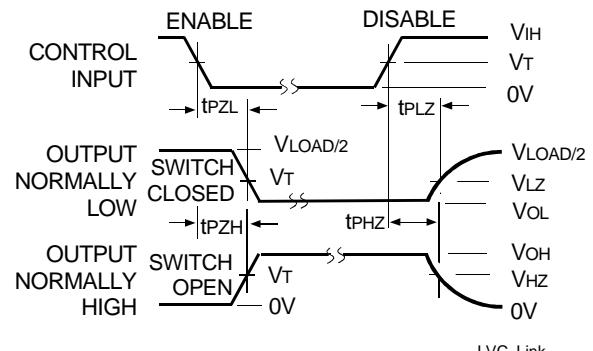
Output Skew -  $t_{SK}(x)$ 

## NOTES:

1. For  $t_{SK}(o)$  OUTPUT1 and OUTPUT2 are any two outputs.
2. For  $t_{SK}(b)$  OUTPUT1 and OUTPUT2 are in the same bank.



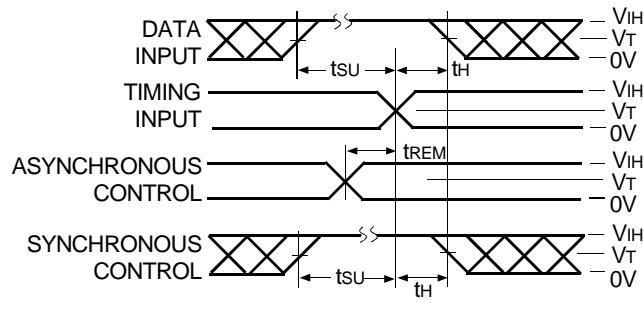
Propagation Delay



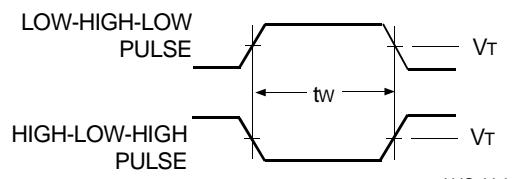
Enable and Disable Times

## NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.



Set-up, Hold, and Release Times



Pulse Width

## ORDERING INFORMATION

IDT	XX	LVC	X	XX	XXXX	XX	
	Temp. Range	Bus-Hold		Family	Device Type	Package	
						PV	Shrink Small Outline Package
						PA	Thin Shrink Small Outline Package
						PF	Thin Very Small Outline Package
					501A		18-bit Registered Transceiver
					16		Double-Density, $\pm 24\text{mA}$
						H	Bus-hold
					74		-40°C to +85°C



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